Shri Shankaracharya Technical Campus,

Shri Shankaracharya Group of Institutions

(An Autonomous Institute affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION

Courses of Study and Scheme of Examination of M. Tech

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

S. No.	Boardof Study	Subject Code	Subject	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1.	Electronics & Telecom	ET231101	VLSI Technology	3	1	-	100	20	20	140	4
2.	Electronics & Telecom	ET231102	VLSI System Design	3	1	-	100	20	20	140	4
3.	Electronics & Telecom	ET231103	MOS Circuit Design	3	1	-	100	20	20	140	4
4.	Electronics & Telecom	ET231104	Modelling with HDLs	3	1	-	100	20	20	140	4
5.	Electronics & Telecom	Refer Table I	Elective – I	3	1	-	100	20	20	140	4
6.	Electronics & Telecom	ET231191	VHDL Modelling Laboratory	-		3	75		75	150	2
7.	Electronics & Telecom	ET231192	Computer Simulation Laboratory	-		3	75		75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table I

Elective-I			
Sr.No.	**Board of Study**	**Subject Code**	**Subject**
1	Electronics & Telecom	ET231121	CMOS RF Circuit Design
2	Electronics & Telecom	ET231122	Real Time System & Software
3	Electronics & Telecom	ET231123	Digital Image Processing

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L-Lecture T- Tutorial P-Practical

CT- Class Test TA- Teachers Assessment ESE- End Semester Exam

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231101	VLSI Technology	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students able to acquire knowledge on semiconductor materialsand their oxidization process and quality measures in the fabrication. The aim is to impart skills to students for explain lithography importance in the semiconductor industry and the various techniques.	On successful completion of the course, the student will be able to: **CO1:-**understands the single crystal development process and the process parameters **CO2:-**analyse the kinetics of oxidization process **CO3:-**analyse the kinetics of oxidization process **CO4:-**understand the lithography importance and various lithographic techniques **CO5:-**understand the basic chemical etching process

UNIT I CRYSTAL GROWTH **C01**

Crystal growth & wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc. Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

UNIT – II SILICON OXIDATION: **CO2**

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2.

UNIT – III DIFFUSION PROCESS: **CO3**

Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

UNIT – IV LITHOGRAPHY: **CO4**

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

UNIT – V ETCHING PROCESS **CO5**

Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching.

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	VLSI Technology	S. M. Sze	2nd Edition	McGraw Hill Book Co
2	"VLSI Fabrication Principles	S.K.Gandhi	2nd Edition	John Wiley and Sons, NY
3	The Science and Engineering of Microelectronic Fabrication	S.A. Campbell	2nd Edition	Oxford

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	VLSI Technology	Chen	3ed Edition	Wiley
2	Principles of Microelectronics Technology	D.Nagchoudhary	2nd Edition	Wheeler (India)

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231102	**VLSI System Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of VLSI system design methodology. Students will be able to understand about physical chip design, hierarchy, memory and memory element design concepts.	On successful completion of the course, the student will be able to: **CO1:-** Outline the features of basics of VLSI system design. **CO2:-** Chip design methods and design capture tools. **CO3:-** Memory and control unit design. **CO4:-** Boolean operations and counter design. **CO5:-** Design of memory elements.

UNIT- I Basics of VLSI System Design: **CO1**

VLSI System Design methodology: Structure Design, Strategy, Hierarchy, Regularity, Modularity, Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design.

UNIT–II **CO2**

Chip Design Methods and capture tools : Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System. HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

UNIT – III Subsystem Designs : **CO3**

Data Path Sub System Design: Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations. SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays.mFinite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.

UNIT – IV CMOS Subsystem Design: **CO4**

CMOS Subsystem Design: Basic theory of CMOS (detail) – Data path operations –Parity generator – Comparators – Zero/one detectors- Binary counters – Boolean operations – Multiplication – Shifters. **[5Hrs]**

UNIT – V Memory Elements: **CO5**

Read/write memory: - RAM- Register files – FIFOs, LIFOs, SIPOs- Serial Access memory. Read only memory – Content Addressable memory - Finite – State Machine – FSM Design procedure – Control Logic implementation: - PLA Control implementation – ROM Control implementation – Multilevel logic – An example of control logic implementation.

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Principles of CMOS VLSI Design	N.H.E.Weste and K.Eshraghian	Second	Addition Wesley,1993
2	Digital Integrated Circuits a design perspective	Jan .M.Rabaey	First	PHI 1st Edition, 1995

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	Principles of CMOS VLSI design	Weste and Eshraghian	Second	Addison-Wesley, 2002
2	CMOS VLSI Design	Wolf	Second	pearson

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI DESIGN)

Subject Code ET231103	**MOS Circuit Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **MOS CIRCUIT DESIGN**. The aim is to impart skills to students for developing and hosting Analog and digital circuit establishment.	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of basics of MOS. **CO2:-** Design layout MOS circuit. **CO3:-** Design structure of Combinational MOS Logic Design. **CO4:-** Design structure of Sequential MOS Logic Design **CO5:-**Learn the structure of BiCMOS Logic Circuits .

UNIT- I Introduction: **CO1**

Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design. The MOS Inverter: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption.

UNIT–II MOS Circuit Layout & Simulation: **CO2**

MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation .

UNIT – III Combinational MOS Logic Design **CO3**

Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits. Dynamic MOS design: Dynamic logic families and performances.

UNIT – IV **CO4**

Sequential MOS Logic Design Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design

Interconnect & Clock Distribution Interconnect delays, Cross Talks, Clock Distribution. Introduction to low power design, Input and Output Interface circuits.

UNIT – V **CO5**

BiCMOS Logic Circuits

Introduction, BJT Structure & operation, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits, BiCMOS Applications

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	CMOS Digital IC Circuit Analysis & Design	Kang & Leblebigi	Second	McGraw Hill
2	Digital Integrated Circuits Design	Rabey	Second Edition	Pearson Education

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	Principles of CMOS VLSI design	Weste and Eshraghian	Second	Addison-Wesley
2	CMOS VLSI Design	Wolf pearson	-	Pearson Education

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics &Telecommunication (VLSI Design)

Subject Code :- ET231104	**Modelling with HDLs**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the**Programming skills in Xilinx along with various operaters and advanced Xilinx progamming cells array**, and it is also help ful for the students to know various different routing schemes.	On successful completion of the course, the student will be able to: **CO1:-**Outline the features study of Various advanced PLDs and FPGAs **CO2:-**learn various Placement and Routing Schemes of circuits. **CO3:-**Understand the basics of hardware description Language. **CO4**:-Understand various modelling Techniques and programming of xilinx **CO5:-**Learn the second hardware description Language verilog.

UNIT-IIntroduction to PLDs & FPGAs : **CO1**

ROMs, Logic array (PLA), Programmable array logic, GAL,bipolar PLA, NMOS PLA, PAL 14L4,Xilinx logic cell array (LCA) – I/O Block – Programmableinterconnect – Xilinx – 3000 series and 4000series FPGAs. Altera CPLDs, altera FLEX 10Kseries PLDs

UNIT–II Placement and routing : **CO2**

Mincut based placement – iterative improvement placement– Routing:Segmented channel routing – Maze routing – Routability and routing resources – Net delays.

UNIT – III Introduction to VHDL : **CO3**

Digital system design process – Hardware simulation – Levels ofabstraction – VHDLrequirements – Elements of VHDL – Top down design VHDL operators –Timing – Concurrency –Objects and classes – Signal assignments – Concurrent and sequentialassignments.

UNIT – IV Structural, Data flow &Behavioral description of hardware in VHDL: **CO4**

Parts library – Wiring ofprimitives – Wiring of iterative networks – Modeling a test bench – Top down wiring

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Chairman(AC)	Chairman (BoS)	Date of Release	Version	

components –Subprograms. Multiplexing and data selection – State machine descriptions – Open collectorgates – Three state bussing. - Process statement – Assertion statement – Sequential waitstatements – Formatted ASCII I/O operations MSI based design.

UNIT – V Introduction to Verilog HDL : CO5

Lexical conventions – Data types – System tasks and CompilerDirectives- Modules and Ports-Gate Level Modeling with Examples.

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	"Digital Design sing Field Programmable Gate Array"	P.K. Chan & S. Mourad,	first	Prentice Hall, 1994.
2	" Field Programmable Gate Array"	J. V. Old Field & R.C. Dorf,	Eight	John Wiley, 1995.

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	" Digital System Design with Programmable Logic"	M. Bolton	Fourth	Addison Wesley, 1990.
2	" VLSI Engineering"	Thomas E. Dillinger	Second	Prentice Hall,1998
3	"VHDL"	Douglas Perry	Third	McGraw Hill 2001.

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231121	**CMOS RF Circuit Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand about the CMOS RF Circuit Design techniques. Students will be able to learn about the transformation, enhancement, restoration, compression, segmentation and representation techniques and methods of CMOS RF Circuit Design.	On successful completion of the course, the student will be able to: **CO1:-** Basic elements in RF Circuit Design. **CO2:-** Transformation techniques of networks. **CO3:-** Enhancement and restoration technique of BJT and MOSFET Behavior at RF Frequencies. **CO4:-** Designs of RF circuit. **CO5:-**Design of Oscillator and Mixers.

UNIT 1

Introduction to RF design and Wireless Technology: Importance of Radio frequency Design, Dimensions and Units, Frequency Spectrum, RF behavior of Passive Component, High frequency resistor, High-frequency capacitors, High-frequency inductors, Chip Components and circuit board Considerations, Chip resistors, Chip capacitors, Surface-mounted inductors.

UNIT 2

Single and Multiport Networks: Basic definitions interconnecting networks, Series connection of networks , Parallel connection of networks , Cascading of networks, Summary of ABCD network representations , Network properties and applications , Interrelation between parameter sets , Analysis of microwave amplifier , Scattering parameters , Definition of scattering parameters, Meaning of S-Parameters , Chain scattering matrix, Conversion between Z-and S- parameters, Signal flow chart modeling, Generalization of S-parameters, Practical measurements of SParameters.

UNIT 3

BJT and MOSFET Behavior at RF Frequencies

BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT 4

RF Circuits Design

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF

systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers,
Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

UNIT 5

Oscillator and Mixers: Basic oscillator model, Negative resistance oscillator, Feedback oscillator design, Design steps, Quartz oscillators, High frequency oscillator, configuration, Fixed frequency oscillators, Dielectric resonator oscillator, YAGI-tuned oscillator, Voltage control oscillator, GUNN element oscillators, Basic characteristics of mixers, Basic concepts, Frequency domain considerations, Single ended mixers design , Double -Balanced mixer.

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	RF Circuit Design Theory and applications	Reinhold Ludwig Pavel Bretchko	First	Pearson
2	Design of CMOS RF Integrated Circuits	Thomas H. Lee	Second	Cambridge University Press

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	RF Microelectronics	B. Razavi	Second	PHI
2	CMOS Circiut Design, layout and Simulation	R. Jacob Baker, H.W. Li, D.E. Boyce	First	PHI

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231122	**Real Time System & Software**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand about the Real Time System & Software techniques. Students will be able to learn about the transformation, enhancement, restoration, compression, segmentation and representation techniques and methods of Real Time System & Software.	On successful completion of the course, the student will be able to: **CO1:-** Basic elements Real Time System & Software. **CO2:-**learn various Requirements and Design Specifications. **CO3:-**Understand the basics of Measurement of Software. **CO4**:-Understand Programming Languages **CO5:-**Learn the Operating Systems.

UNIT 1

Introduction, Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues. Process and State-based Systems model, Periodic and Sporadic Process, Cyclic Executives, CE definitions and Properties, Foreground-Background Organiazations, Standard OS and Concurrency – Architectures, Systems Objects and Object- Oriented Structures, Abstract Data Types, General Object Classes.

UNIT 2

Requirements and Design Specifications: Classification of Notations, Data Flow Diagrams, Tabular Languages, State Machine, Communicating Real Time State Machine- Basic features, Timeing and clocks, Sementics Tools and Extensions, Statecharts-Concepts and Graphical Syntax, Semantics and Tools Declarative Specifications: Regular Expressions and Extensions, Traditional Logics-Propositional Logic, Predicates, Temporal logic, Real time Logic Deterministic Scheduling : Assumptions and Candidate Algorithms, Basic RM and EDF Results, Process Interactions-Prority Inversiotn and Inheritance.

UNIT 3

Execution Time Prediction: Measurement of Software by software, Program Analysis with Timing Schema, Schema Concepts, Basic Blocks, Statements and Control, Schema Practice, Prediction by optimisation, System Interference and Architectural ComplexitiesTimer Application, Properities of Real and ideal clocks, Clock Servers – Lamport's Logical clocks, Monotonic Clock service, A software Clock server, Clock Synchronization- Centralized Synchronization, Distributed Synchronization

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UNIT 4

Programming Languages: Real Time Language Features, Ada-Core Language, Annex Mechanism for Real Time Programming, Ada and Software Fault Tolerance, Java and Real-time Externsions, CSP and Occam

UNIT 5

Operating Systems: Real Time Functions and Sevices, OS Architectures-Real Time UNIX and POSIX, Issues in Task management- Processes and Threads, Scheduling, Synchronization and communication

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Real – Time Systems and software	Alan C. Shaw	First	John Wiley & Sons Inc

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231123	**Digital Image Processing**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand about the image processing techniques. Students will be able to learn about the transformation, enhancement, restoration, compression, segmentation and representation techniques and methods of images.	On successful completion of the course, the student will be able to: **CO1:-** Basic elements in image processing. **CO2:-** Transformation techniques of images using FFT. **CO3:-** Enhancement and restoration technique of images. **CO4:-** Image compression and segmentation techniques. **CO5:-**Representation, coding, recognition and Interpretation methods.

UNIT- I Digital Image Fundamentals: **CO1**

Introduction And Digital Image Fundamentals: Digital Image Representation, Fundamental Steps in Image Processing, Elements of Digital image processing systems, Sampling and quantization, some basic relationships like neighbours, connectivity, Distance measure between pixels, Imaging Geometry.

UNIT–II Image Transforms: **CO2**

Discrete Fourier Transform, Some properties of the two-dimensional fourier transform, Fast fourier transform, Inverse FFT.

UNIT – III Image Enhancement and Restoration : **CO3**

Spatial domain methods, Frequency domain methods, Enhancement by point processing, Spatial filtering, Lowpass filtering, Highpass filtering, Homomorphic filtering, Colour Image Processing. Degradation model, Diagnolization of Circulant and Block-Circulant Matrices, Algebraic Approach to Restoration, Inverse filtering, Wiener filter, Constrained Least Square Restoration, Interactive Restoration, Restoration in Spatial Domain.

UNIT – IV Image Compression and Segmentation: **CO4**

Coding, Interpixel and Psychovisual Redundancy, Image Compression models, Error free comparison, Lossy compression, Image compression standards. Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation.

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UNIT – V Representation, Recognition, andInterpretation: **CO5**

Representation schemes like chain coding, Polygonal Approximatiion, Signatures, Boundary Segments, Skeleton of region, Boundary description, Regional descriptors, Morphology. Elements of Image Analysis, Pattern and Pattern Classes, Decision-Theoretic Methods, Structural Methods, Interpretatiion.

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Digital Image Processing	Rafael C. Conzalez & Richard E. Woods	Fifth	Pearson
2	Fundamental of Digital Image Processing	A.K. Jain	First	Prentice Hall, 1989

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	Digital Picture Processing	Rosefield Kak	Second	Computer Science and Scientific Computing
2	Digital Image Processing	W.K. Pratt	Fourth	A John Wiley & Sons, Inc., Publication

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231191	**VHDL Modelling Laboratory**	**L = 0**	**T = 0**	**P = 3**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	75	**-**	**75**	**150**	**3 Hours**

List of Experiments using VHDL

01 Half adder, Full adder, Subtractor Flip Flops, 4bit comparator.

02 Parity generator

03 Bit up/down counter with load able count

04 Decoder and encoder

05 8 bit shift register

06 8:1 multiplexer

07 Test bench for a full adder

08 Barrel shifter

09 N by m binary multiplier

10 RISC CPU (3bit opcode, 5bit address)

TOOLS:
Xilinx Tools, Cadence Tools, Model SIM, Leonardo Spectrum Tools shall be used.

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SCHEME OF EXAMINATION AND SYLLABUS

1st Semester M. Tech. Electronics & Telecommunication (VLSI Design)

Subject Code ET231192	**Computer Simulation Laboratory**	**L = 0**	**T = 0**	**P = 3**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	75	**-**	**75**	**150**	**3 Hours**

List of Experiments

1. SPICE simulation of basic analog circuits.

2. Analog Circuit simulation using labview tools

3. Verification of layouts (DRC, LVS)

4. Back annotation

Tools used : Cadence tools, Mentor Graphics tools, lab view tools, multisim

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